

32. (Twice Amended) A capacitor structure comprising:

a first electrode;

a high dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a chemical vapor deposited diffusion barrier layer formed of RuSi_x , where x is in the range of about 0.01 to about 10.

36. (Twice Amended) A integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region;

and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a chemical vapor deposited diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of RuSi_x , where x is in the range of about 0.01 to about 10.

39.(New) The structure of claim 27, wherein the surface of the substrate assembly defines an opening, where the diffusion barrier layer is on the surface defining the opening.

40.(New) The structure of claim 39, wherein the opening has an aspect ratio greater than about 1.

41.(New) The structure of claim 39, wherein the diffusion barrier layer comprises a conformal layer within the opening.

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For: DEVICE STRUCTURES INCLUDING RUTHENIUM SILICIDE DIFFUSION BARRIER LAYERS

42.(New) The capacitor structure of claim 32, wherein the capacitor structure includes a surface defining an opening, and where a diffusion barrier layer is on the surface defining the opening.

43.(New) The capacitor structure of claim 42, wherein the opening has an aspect ratio greater than about 1.

44.(New) The capacitor structure of claim 43, wherein the diffusion barrier layer comprises a conformal layer of uniform thickness within the opening.